SDSU | College of Engineering Mechanical Engineering

Mechanical Engineering Seminar Series

September 22, 2026,11:00AM

Dean's Conference Room, E 203E

Title: Engineering Challenges in Advanced Semiconductor Packaging and High-Performance Semiconductor Chips

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Abstract: The rapid evolution of nanoelectronics has been driven for decades by transistor scaling, enabling continued improvements in performance, integration, and cost. As conventional scaling approaches their physical and economic limits, Moore's Law has increasingly shifted toward advanced semiconductor packaging and heterogeneous integration. However, the growing complexity of AI and high-performance computing (HPC) systems is revealing new challenges that extend well beyond interconnect density. As packages become larger, thinner, and increasingly heterogeneous, critical issues such as warpage, glass fragility, hybrid-bonding yield, temporary-bonding variability, and substrate limitations are emerging as key barriers to further advancement. These challenges highlight a fundamental shift in the industry: the primary roadblocks are no longer purely electrical, but increasingly involve the coordinated integration of materials, mechanical behavior, thermal processes, manufacturing variability, and yield management. This talk will provide an overview of the current state of advanced semiconductor packaging and high-performance semiconductor chips, focusing on emerging technical challenges, process-integration requirements, and opportunities for next-generation applications. Particular attention will be given to how advances in packaging technologies can enable continued scaling of AI, HPC, and other demanding computing systems.

Bio: Dr. Park is a professor at the School of Electrical, Computer and Biomedical Engineering at the University of Nevada, Reno (UNR), NV, USA. He joined UNR in July 2019. Before that, he was an Associate Professor in the School of Electrical Engineering and Computer Science at the University of Ottawa, Canada (2016-2021; currently Adjunct Professor) and a scientist at SLAC National Accelerator Laboratory, Stanford University, USA (2014-2016). For six years (2008-2014), he served as a senior technologist to support the corporate chief technology officer (CTO) and business units at Applied Materials, USA. In addition, he has been a guest researcher at the Lawrence Berkeley National Laboratory (2005-2008), an adjunct professor in the Department of Electrical Engineering at Santa Clara University (2009-2016), and a visiting scholar in the Department of Electrical Engineering at Stanford University, CA, USA (2013-2014). He received his Ph.D. (2008) in materials science and engineering from the University of California, San Diego, USA. He is a senior member of IEEE and the National Academy of Inventors.